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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/603,055 | 06/24/2003 | Gianluca Blasi | 32079-00087USPX | 8552 |

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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/603,055 | BLASI ET AL. | |
| | Examiner | Art Unit | |
| | Mary C. Jacob | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-28 have been presented for examination.

### *Drawings*

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 365.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 210, 354, 355, 356, 357, 358, 559, 614, 657, and 658. Further, Figures 4a-4h are only mentioned in the description as Figure 4 and are not described.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

4. Claim 6 objected to because of the following informalities. Appropriate correction is required.

5. Claim 6, line 2, the word "input" is spelled incorrectly.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3, 6-8, 10, 15, 16, 19, 21, 22, 23, 26, 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al ("A Goal Tree Based High-Level Test Planning System for DSP Real Number Models", Proceedings of the International Test Conference, pages 1000-1009, October 18-23, 1998).

8. As to Claims 1, 8, Lin et al teaches: a computer based test bench generator for verifying integrated circuits specified by models in a Hardware Description Language, comprising: a repository storing a general set of self-checking tests applicable to integrated circuits (section 2, lines 14-16; section 4.1, paragraph 5); means for entering behavior data of an integrated circuit model (section 3, paragraph 2, lines 2-5); means for entering configuration data of the integrated circuit model (section 6); means for automatically generating test benches in said Hardware Description Language, said means being configured to make a selection and setup of suitable tests from said

repository according to the specified integrated circuit model, configuration and behavior data (section 2, lines 22-29; section 3, paragraph 1, lines 1-3; section 6).

9. As to Claims 15 and 22, Lin et al teaches: a test bench generator for integrated circuit designs, comprising: a repository which stores functional and structural characteristic data for integrated circuit models (Figure 1, VHDL Primitive Library, Specification Repository); a processing functionality which receives an identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model, the processing functionality operating to: process the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation; and compare the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model (section 2, lines 10-29; section 3, paragraphs 1 and 2; section 4.1, paragraph 5; Figure 6 and description).

10. As to Claims 3 and 10, Lin et al teaches: wherein said general set of tests is specified in said Hardware Description Language (section 3, paragraph 1, lines 1-3).

11. As to Claim 6, Lin et al teaches: wherein said configuration data is input to said generator through a command line (Figures 4-6).

12. As to Claim 7, Lin et al teaches: wherein said selection of tests is based on conditional statements (page 1004, first 2 lines, item 3; Figure 7).

13. As to Claims 16 and 23, Lin et al teaches: wherein the processing functionality further processes the identified tests which are applicable to produce a set of self-

checking test benches for the specific integrated circuit model (section 2, lines 26-27; Figure 1, "VHDL Simulator").

14. As to Claims 19 and 26, Lin et al teaches: wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested, are specified using a hardware description language (section 2, lines 11-15, lines 22-25; section 3, paragraph 2, lines 2-5).

15. As to Claim 21, Lin et al teaches: further including a simulator functionality which applies the identified applicable tests against the configured integrated circuit model (section 2, lines 26-27; Figure 1, "VHDL Simulator").

16. As to Claim 28, Lin et al teaches: further including applying the identified applicable tests against the configured integrated circuit model to simulate operation (section 2, lines 26-27; Figure 1, "VHDL Simulator").

### *Claim Rejections - 35 USC § 103*

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 2, 4, 5, 9, 11-14, 17, 20, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al as applied to claims 1. 8. 15 and 22 above, in view of Bollano et al ("The Virtual Intellectual Property Library: From Paradigm to Product", Proc. Of IP99 Conference, Santa Clara, March 1999).

20. As to Claims 2, 4, 5, 9, 11-14, 17, 20, 24 and 27, Lin et al teaches a test bench generator for verifying integrated circuits wherein the hardware description language is VHDL (section 2, lines section 3, paragraph 1, lines 1-3; section 3, paragraph 2, lines 2-5); wherein said configuration data is input to said generator through a command line (Figures 4-6); wherein said configuration data is input to said generator through a command line (Figures 4-6).

21. Lin et al does not expressly teach: wherein the integrated circuit model is a memory model, wherein the hardware description language can be Verilog, or wherein said behavior data is specified in proprietary language.

22. Bollano et al teaches a system that implements a soft IP library in the design flow to shorten the design time and lower the design cost by making system know-how available as customizable, reliable and reusable design blocks through the use of a Virtual Intellectual Properties library that is composed of system level modules written in VHDL (page 1, column 1), wherein said integrated circuit model is a memory model

(page 3, column 2, lines 5-8); wherein said hardware description language can be VHDL or Verilog (page 4, column 2, last paragraph, first sentence); wherein said behavior data is specified in proprietary language (pages 4-5, "IP Code Protection") and wherein the user can set up scenario and parameter values through a menu for use of the modules and functional verification and validation is carried out through RTL simulation using the VIP test bench modules for pattern generation and response analysis (page 3, column 2, "Simulation, verification and characterization").

23. Lin et al and Bollano et al are analogous art because they are both directed to the testing and validation of integrated circuits defined in a hardware description language using test benches.

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the integrated circuit model as defined by Lin et al with a memory model, Verilog code or proprietary language as taught by Bollano et al since Bollano et al teaches a system that implements a soft IP library in the design flow to shorten the design time and lower the design cost by making system know-how available as customizable, reliable and reusable design blocks through the use of a Virtual Intellectual Properties library that is composed of system level modules written in VHDL (page 1, column 1).

25. Claims 18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al as applied to Claims 15 and 22 above, in further view of Killian et al (U.S. Patent 6,477,683).

26. As to Claims 8 and 25, Lin et al teaches a test bench generator for integrated circuit designs wherein the processing functionality further processes the identified tests which are applicable to produce a set of self-checking test benches for the specific integrated circuit model (section 2, lines 26-27; Figure 1, "VHDL Simulator").

27. Lin does not expressly teach wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

28. Killian et al teaches a method that automatically configures a processor by generating both a description of a hardware implementation of the processor in HDL and a set of development tools such as a compiler, assembler, debugger and simulator for programming the processor from the same configuration specification (column 6, lines 32-60), which allows for a complete flow for configuration of processor hardware and software including feedback from hardware design results and software performance to aid selection of optimal configuration for the design instead of hardware and software configuration alone (column 8, lines 54-61). The method taught by Killian et al includes a test bench for integrated circuit designs that incorporates complex constructs for comparing data (column 33, lines 25-27), waiting for internal events (column 33, lines 56-59; column 34, lines 61-62), and timing constraint checking with respect to the specific integrated circuit model (column 23, lines 14-17, lines 34-40, lines 48-50).

29. Lin et al and Killian et al are analogous art because they are both directed to the design and verification of integrated circuit designs described in HDL using a test bench.

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the test benches as taught in Lin et al to include constructs for comparing data, waiting for internal events and checking timing constraints as taught by Killian et al since Killian et al teaches a method that allows for a complete flow for configuration of processor hardware and software including feedback from hardware design results and software performance to aid selection of optimal configuration for the design instead of hardware and software configuration alone (column 8, lines 54-61).

***Conclusion***

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

32. Casavant et al (U.S. Patent 6,975,976) teaches generating property-specific test benches.

33. Fields et al (U.S. Patent 6,904,397) teaches developing a reusable electronic circuit design module wherein design elements are stored in a database and the design is simulated with a test bench.

34. Bloom et al (U.S. Patent 6,513,143) teaches a computer implemented apparatus and method that automates the entry, modification, analysis, and generation of test

benches from electrical circuits, both of which are specified as hardware description language (HDL) files.

35. McNamara et al (U.S. 6,687,662) teaches a system and method for automated design verification including the simulation using a test bench.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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